```
RCS file: /s6/cvsroot/euterpe/BOM,v
Working file: BOM
head: 5.105
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1940;  selected revisions: 17
description:
top level BOM
----------------------------
revision 3.565
date: 1995/04/06 23:00:24;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc


Picked up placement BOMs and bug fixes as described below.
Have run 5woody in verilog simulation.


RCS file: /p/cvsroot/euterpe/verilog/bsrc/euterpe.V,v
revision 6.392
date: 1995/04/06 14:54:55 LT;  author: billz;  state: Exp;  lines: +4 -2
Added interface signal hz10or12back (HZ-something-or-other) to
cc.  Consistant with cc v1.77.

----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/uu/uuprblmr9.Veqn,v
RCS file: /p/cvsroot/euterpe/verilog/bsrc/uu/uu.V,v

revision 61.15
date: 1995/04/05 13:35:16 LT;  author: mws;  state: Exp;  lines: +13 -9
uu/uuprblmr9 uu/uu.V:  uuYieldsNbInR10 was on for Ifetch loopbacks, allowing
  CC to make new fill requests to NB and thus discarding loopbacks in progress.
  Test cachenasty3 accidentally noticed on a SN128WrtI.

----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/uu/uursrvduv.pla,v
revision 170.2
date: 1995/04/06 12:37:12 LT;  author: mws;  state: Exp;  lines: +2 -2
Unclosed comment lost EDepI/EWithdrawI check for both
  immediates > 31.  Found by veena test uu/edepi.pl.

----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/cc/ccseq.Veqn,v
revision 28.19
date: 1995/04/06 11:22:53 LT;  author: billz;  state: Exp;  lines: +2 -2
Corrected arc to oblivion in ccseq.Veqn.  Saved one atom.
----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/cc/cc.V,v
RCS file: /p/cvsroot/euterpe/verilog/bsrc/cc/cclatedirty.Veqn,v

revision 1.77
date: 1995/04/06 14:29:13 LT;  author: billz;  state: Exp;  lines: +24 -5
Adds the "cache index match 12 back" case to be a latedirty
case.  That is if a clean miss occurs and there happened to
```

```
be a store to the same cache line 12 cycles back, it turns
into a dirty miss, and the cache line is written back.

Caution: cc interface changes.  hz10or12backR5R6 signal added.

Haven't update placement yet; add the moment, need a gplace license.
Haven't updated euterpe yet, but will.

This problem brought to light in cachenasty2.
----------------------------------------
----------------------------
revision 3.564
date: 1995/04/06 21:55:54;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

change shape of placement - holein bottom right corner
----------------------------
revision 3.563
date: 1995/04/06 21:40:19;  author: tom;  state: Exp;  lines: +2 -2
Release Target: euterpe/compass
      vlsi.boo-all
      vlsi.boo-dcell
      vlsi.boo-tapeout

change library name from euterpelocked to euterpe
----------------------------
revision 3.562
date: 1995/04/06 06:45:50;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc

move placement right and redo center control stipe to solve un-routes
----------------------------
revision 3.561
date: 1995/04/06 06:40:41;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

elliminate placement collisions
----------------------------
revision 3.560
date: 1995/04/06 06:37:31;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/es

move horizontal squeezing
----------------------------
revision 3.559
date: 1995/04/06 01:09:41;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cc

Check in of new placement.  58 rows. Aligned to
nb, at, and sr.  Converges in 0 iterations.

Note: this placement is generated from pimlib.pl.
And includes pla.pim and cc_misc.pim files.
----------------------------
revision 3.558
date: 1995/04/05 21:11:28;  author: fwo;  state: Exp;  lines: +2 -2
Release Target: euterpe/compass/layouts
```

```
Removed bogus and incorrectly placed pad from
proteus/compass/layouts/stpadcorner.ly into steuterpe1padtl.ly
and steuterpe1padtr.ly.
----------------------------
revision 3.557
date: 1995/04/04 18:51:52;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

100% handplace hc1
----------------------------
revision 3.556
date: 1995/04/04 18:14:36;  author: brian;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/standalone/hc

Added changes for new hc event register access.
----------------------------
revision 3.555
date: 1995/04/04 05:14:06;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

move control to center - saves 400 atoms
----------------------------
revision 3.554
date: 1995/04/04 00:28:04;  author: geert;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cp

New placement. Made space for VDDTS

Geert
----------------------------
revision 3.553
date: 1995/04/03 23:42:41;  author: geert;  state: Exp;  lines: +2 -2
Release Target: euterpe/compass/layouts
      euterpe-hwc.ly

New obstruction mask

Geert
----------------------------
revision 3.552
date: 1995/04/03 20:15:10;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

moved pc to bit positions 63:0 from 127:64 and moved bypass mux elements to free
up more horizontal tracks
----------------------------
revision 3.551
date: 1995/04/03 17:44:10;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gf

moved to align with bit positions 127:64 instead of 63:0
----------------------------
revision 3.550
date: 1995/04/03 07:16:16;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc
```

```
uu/uursrvduu.tdcd cj/Makefile:
  Typo's left out GShuffleI4Mux (ex15test_0) and merge deposits
  (exresemdepitest1_0 and exresgmdepitest1_0).   Add rsrvdgsffli4mx.tst rule.
yy/tas.pl:  Typo's prevented shufflei4mux from being recognized.
----------------------------
revision 3.549
date: 1995/04/02 02:55:28;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

uu/uursrvduu.tdcd cj/rsrvd.tst Makefile:
  Typo left GCompressI out of the care sets and it then tended to become a
  reserved instruction (noticed by test xlu_subset_r1_1).
  Typo left GShuffleI and GShuffleI4Mux not checking their immediates (noticed
  by test ex15test_0).  Add rsrvdgshffli.tst rule.
tst/drvchk.V ife/ifetst.tst cj/cjrst.tst:
  Compatible with recent mem mngmnt pipelining.
tst/job.tst:  Comment out perl debug warnings.
ife/iffree.tst:  Experiments preparing for change in reset vector.
euterpe.status:
  Add note on LTLB changing under IFetch violating protection at new GVA.
  Remove note about lack of pipelined memory management enable.
  Add note on writeback reject bug worries.
  Add note on ICache size change exposure with mem management mode change.
Makefile euterpe_wrap.V i_euterpe_wrap.tb i_euterpe_wrap.vhdl:  lisar stuff.
=============================================================================

RCS file: /s6/cvsroot/euterpe/baseplate/membrane.lst,v
Working file: baseplate/membrane.lst
head: 15.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 15.1
date: 1995/04/05 16:17:46;  author: lisar;  state: Exp;
Document the membrane probe card
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/BOM,v
Working file: compass/BOM
head: 7.21
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 67;    selected revisions: 3
description:
----------------------------
revision 3.7
date: 1995/04/06 21:39:55;  author: tom;  state: Exp;  lines: +4 -4
Release Target: euterpe/compass
      vlsi.boo-all
      vlsi.boo-dcell
      vlsi.boo-tapeout
```

```
change library name from euterpelocked to euterpe
----------------------------
revision 3.6
date: 1995/04/05 21:11:12;  author: fwo;  state: Exp;  lines: +2 -2
Release Target: euterpe/compass/layouts

Removed bogus and incorrectly placed pad from
proteus/compass/layouts/stpadcorner.ly into steuterpe1padtl.ly
and steuterpe1padtr.ly.
----------------------------
revision 3.5
date: 1995/04/03 23:42:17;  author: geert;  state: Exp;  lines: +2 -2
Release Target: euterpe/compass/layouts
      euterpe-hwc.ly

New obstruction mask

Geert
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/vlsi.boo-all,v
Working file: compass/vlsi.boo-all
head: 1.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
.boo file listing all libraries in normal order
----------------------------
revision 1.9
date: 1995/04/06 21:39:28;  author: tom;  state: Exp;  lines: +3 -3
change library name from euterpelocked to euterpe
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/vlsi.boo-dcell,v
Working file: compass/vlsi.boo-dcell
head: 1.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
.boo file listing all libraries, with dcells first
----------------------------
revision 1.8
date: 1995/04/06 21:39:30;  author: tom;  state: Exp;  lines: +3 -3
change library name from euterpelocked to euterpe
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/vlsi.boo-tapeout,v
Working file: compass/vlsi.boo-tapeout
head: 1.11
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
.boo file listing only locked libraries
----------------------------
revision 1.9
date: 1995/04/06 21:39:33;  author: tom;  state: Exp;  lines: +3 -3
change library name from euterpelocked to euterpe
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/BOM,v
Working file: compass/layouts/BOM
head: 27.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 79;    selected revisions: 3
description:
releasebom adding BOM
----------------------------
revision 17.0
date: 1995/04/05 21:11:00;  author: fwo;  state: Exp;  lines: +1 -1
Release Target: euterpe/compass/layouts

Removed bogus and incorrectly placed pad from
proteus/compass/layouts/stpadcorner.ly into steuterpe1padtl.ly
and steuterpe1padtr.ly.
----------------------------
revision 16.2
date: 1995/04/05 21:10:50;  author: fwo;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 16.1
date: 1995/04/03 23:42:05;  author: geert;  state: Exp;  lines: +2 -2
Release Target: euterpe/compass/layouts
      euterpe-hwc.ly

New obstruction mask

Geert
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/euterpe-hwc.ly,v
Working file: compass/layouts/euterpe-hwc.ly
head: 5.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 5.5
date: 1995/04/03 23:41:22;  author: chip;  state: Exp;  lines: +28 -2
```

```
periodic checkin of Mon Apr  3 16:41:20 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/steuterpe1padtl.ly,v
Working file: compass/layouts/steuterpe1padtl.ly
head: 8.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 8.2
date: 1995/04/05 21:03:32;  author: chip;  state: Exp;  lines: +4 -2
periodic checkin of Wed Apr  5 14:03:29 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/steuterpe1padtr.ly,v
Working file: compass/layouts/steuterpe1padtr.ly
head: 8.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 8.2
date: 1995/04/05 21:03:34;  author: chip;  state: Exp;  lines: +4 -2
periodic checkin of Wed Apr  5 14:03:29 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/vlsi.cko,v
Working file: compass/layouts/vlsi.cko
head: 2.73
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 73;    selected revisions: 5
description:
----------------------------
revision 2.23
date: 1995/04/05 21:03:36;  author: chip;  state: Exp;  lines: +0 -2
periodic checkin of Wed Apr  5 14:03:29 PDT 1995
----------------------------
revision 2.22
date: 1995/04/05 19:47:03;  author: chip;  state: Exp;  lines: +1 -0
periodic checkin of Wed Apr  5 12:47:01 PDT 1995
----------------------------
revision 2.21
date: 1995/04/05 19:45:27;  author: chip;  state: Exp;  lines: +1 -0
periodic checkin of Wed Apr  5 12:45:25 PDT 1995
----------------------------
revision 2.20
date: 1995/04/03 23:41:24;  author: chip;  state: Exp;  lines: +0 -1
```

```
periodic checkin of Mon Apr  3 16:41:20 PDT 1995
----------------------------
revision 2.19
date: 1995/04/03 23:24:03;  author: chip;  state: Exp;  lines: +1 -0
periodic checkin of Mon Apr  3 16:24:00 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/vlsi.log,v
Working file: compass/layouts/vlsi.log
head: 2.88
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 88;    selected revisions: 5
description:
----------------------------
revision 2.24
date: 1995/04/05 21:03:37;  author: chip;  state: Exp;  lines: +4 -0
periodic checkin of Wed Apr  5 14:03:29 PDT 1995
----------------------------
revision 2.23
date: 1995/04/05 19:47:04;  author: chip;  state: Exp;  lines: +1 -0
periodic checkin of Wed Apr  5 12:47:01 PDT 1995
----------------------------
revision 2.22
date: 1995/04/05 19:45:29;  author: chip;  state: Exp;  lines: +1 -0
periodic checkin of Wed Apr  5 12:45:25 PDT 1995
----------------------------
revision 2.21
date: 1995/04/03 23:41:25;  author: chip;  state: Exp;  lines: +2 -0
periodic checkin of Mon Apr  3 16:41:20 PDT 1995
----------------------------
revision 2.20
date: 1995/04/03 23:24:05;  author: chip;  state: Exp;  lines: +1 -0
periodic checkin of Mon Apr  3 16:24:00 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/BOM,v
Working file: verify/BOM
head: 12.34
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 404;   selected revisions: 1
description:
----------------------------
revision 4.87
date: 1995/04/04 18:14:12;  author: brian;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/standalone/hc

Added changes for new hc event register access.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/include/physaddr.h,v
Working file: verify/include/physaddr.h
```

```
head: 4.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 24;    selected revisions: 2
description:
----------------------------
revision 4.22
date: 1995/04/06 05:29:57;  author: lisar;  state: Exp;  lines: +13 -4
Fix HERMESINTERLEAVESHIFT
----------------------------
revision 4.21
date: 1995/04/04 22:29:40;  author: jeffm;  state: Exp;  lines: +10 -1
Make event daemon address macros generate addresses at blocking read
offset.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/obj/processor/inst/Makefile,v
Working file: verify/obj/processor/inst/Makefile
head: 1.182
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 182;   selected revisions: 5
description:
----------------------------
revision 1.138
date: 1995/04/06 18:10:36;  author: jeffm;  state: Exp;  lines: +2 -2
Test cached event handler and bbacking to cached code streams.
----------------------------
revision 1.137
date: 1995/04/06 05:40:46;  author: lisar;  state: Exp;  lines: +2 -2
Corrected spelling of nbhilotest
----------------------------
revision 1.136
date: 1995/04/06 00:37:34;  author: jeffm;  state: Exp;  lines: +3 -3
New tests.
----------------------------
revision 1.135
date: 1995/04/04 01:44:40;  author: jeffm;  state: Exp;  lines: +2 -2
cachenasty3 - new test, same as cachenasty2, but with only two lo-prio
nb entries.

dcacheharder7 - fixed to not cause illegal address (but still think
we might get ex11).
----------------------------
revision 1.134
date: 1995/04/04 01:22:12;  author: lisar;  state: Exp;  lines: +4 -3
Added new interleave tests
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/stgen_r16899.S,v
Working file: verify/random/stgen_r16899.S
head: 3.2
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/04/04 01:53:44;  author: lisar;  state: Exp;
More random tests (old stgen)
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/stgen_r17070.S,v
Working file: verify/random/stgen_r17070.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/04/04 01:53:48;  author: lisar;  state: Exp;
More random tests (old stgen)
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/stgen_r17235.S,v
Working file: verify/random/stgen_r17235.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/04/04 01:53:50;  author: lisar;  state: Exp;
More random tests (old stgen)
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/stgen_r17405.S,v
Working file: verify/random/stgen_r17405.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/04/04 01:53:52;  author: lisar;  state: Exp;
More random tests (old stgen)
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/stgen_r22478.S,v
```

```
Working file: verify/random/stgen_r22478.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/04/04 01:46:48;  author: lisar;  state: Exp;
found hermes problem
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/stgen_r29924.S,v
Working file: verify/random/stgen_r29924.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/04/04 01:45:59;  author: lisar;  state: Exp;
 Uses the new stgen
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/BOM,v
Working file: verify/standalone/BOM
head: 6.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 85;    selected revisions: 1
description:
----------------------------
revision 4.25
date: 1995/04/04 18:13:59;  author: brian;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/standalone/hc

Added changes for new hc event register access.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/BOM,v
Working file: verify/standalone/hc/BOM
head: 11.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
```

```
revision 10.0
date: 1995/04/04 18:13:46;  author: brian;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/standalone/hc

Added changes for new hc event register access.
----------------------------
revision 9.1
date: 1995/04/04 18:13:37;  author: brian;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/NOTES,v
Working file: verify/standalone/hc/NOTES
head: 1.28
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 28;    selected revisions: 1
description:
----------------------------
revision 1.24
date: 1995/04/04 17:59:00;  author: brian;  state: Exp;  lines: +18 -0
Modified for new event handling. Hc now pases lower bits to allow access
to all event daemon registers.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/event.pl,v
Working file: verify/standalone/hc/event.pl
head: 5.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 5.3
date: 1995/04/04 19:43:11;  author: woody;  state: Exp;  lines: +5 -31
Update to include design change and to use hclib.pl for subroutines.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/evnt8.vec,v
Working file: verify/standalone/hc/evnt8.vec
head: 5.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 5.7
date: 1995/04/04 17:59:03;  author: brian;  state: Exp;  lines: +8 -8
Modified for new event handling. Hc now pases lower bits to allow access
to all event daemon registers.
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/hclib.pl,v
Working file: verify/standalone/hc/hclib.pl
head: 9.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 9.1
date: 1995/04/04 19:41:58;  author: woody;  state: Exp;
A collection of subroutines for generating nbhc standalone tests.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/nbhc_drive.V,v
Working file: verify/standalone/hc/nbhc_drive.V
head: 1.55
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 55;    selected revisions: 1
description:
----------------------------
revision 1.47
date: 1995/04/04 17:59:05;  author: brian;  state: Exp;  lines: +11 -11
Modified for new event handling. Hc now pases lower bits to allow access
to all event daemon registers.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/nb/NOTES,v
Working file: verify/standalone/nb/NOTES
head: 1.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16;    selected revisions: 1
description:
----------------------------
revision 1.13
date: 1995/04/04 18:17:22;  author: brian;  state: Exp;  lines: +4 -1
Update of NOTES.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/nb/vecgen.c,v
Working file: verify/standalone/nb/vecgen.c
head: 1.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
```

```
revision 1.9
date: 1995/04/04 18:14:57;  author: brian;  state: Exp;  lines: +4 -4
Changed event 'a' arm command to use 0x8 instead of 0x0 in lower portion
of address.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/tools/stgen,v
Working file: verify/tools/stgen
head: 5.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 2
description:
----------------------------
revision 5.9
date: 1995/04/07 00:20:09;  author: doi;  state: Exp;  lines: +8 -3
include information on how to rerun a particular test in the output
----------------------------
revision 5.8
date: 1995/04/03 16:31:35;  author: doi;  state: Exp;  lines: +7 -7
fixed typo that prevented hermes channels from being enabled
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Makefile,v
Working file: verify/toplevel/Makefile
head: 1.185
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 185;   selected revisions: 5
description:
----------------------------
revision 1.138
date: 1995/04/06 18:10:36;  author: jeffm;  state: Exp;  lines: +2 -2
Test cached event handler and bbacking to cached code streams.
----------------------------
revision 1.137
date: 1995/04/06 05:40:46;  author: lisar;  state: Exp;  lines: +2 -2
Corrected spelling of nbhilotest
----------------------------
revision 1.136
date: 1995/04/06 00:37:34;  author: jeffm;  state: Exp;  lines: +3 -3
New tests.
----------------------------
revision 1.135
date: 1995/04/04 01:44:40;  author: jeffm;  state: Exp;  lines: +2 -2
cachenasty3 - new test, same as cachenasty2, but with only two lo-prio
nb entries.

dcacheharder7 - fixed to not cause illegal address (but still think
we might get ex11).
----------------------------
revision 1.134
date: 1995/04/04 01:22:12;  author: lisar;  state: Exp;  lines: +4 -3
```

```
Added new interleave tests
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/brimmlongtest.S,v
Working file: verify/toplevel/brimmlongtest.S
head: 35.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 35.1
date: 1995/04/06 00:37:24;  author: jeffm;  state: Exp;
New tests.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/brimmlongtest2.S,v
Working file: verify/toplevel/brimmlongtest2.S
head: 35.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 35.1
date: 1995/04/06 00:37:28;  author: jeffm;  state: Exp;
New tests.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Attic/cachenasty3.S,v
Working file: verify/toplevel/cachenasty3.S
head: 35.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 35.1
date: 1995/04/04 01:44:34;  author: jeffm;  state: Exp;
cachenasty3 - new test, same as cachenasty2, but with only two lo-prio
nb entries.

dcacheharder7 - fixed to not cause illegal address (but still think
we might get ex11).
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/dcacheeasy.S,v
Working file: verify/toplevel/dcacheeasy.S
head: 11.13
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 1
description:
----------------------------
revision 11.13
date: 1995/04/06 22:12:41;  author: jeffm;  state: Exp;  lines: +4 -4
Fix test bugs.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/dcacheharder4.S,v
Working file: verify/toplevel/dcacheharder4.S
head: 31.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 31.3
date: 1995/04/06 22:12:44;  author: jeffm;  state: Exp;  lines: +2 -2
Fix test bugs.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/dcacheharder7.S,v
Working file: verify/toplevel/dcacheharder7.S
head: 35.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 35.2
date: 1995/04/04 01:44:37;  author: jeffm;  state: Exp;  lines: +24 -18
cachenasty3 - new test, same as cachenasty2, but with only two lo-prio
nb entries.

dcacheharder7 - fixed to not cause illegal address (but still think
we might get ex11).
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/ex11test3.S,v
Working file: verify/toplevel/ex11test3.S
head: 35.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 35.1
date: 1995/04/06 00:37:31;  author: jeffm;  state: Exp;
New tests.
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/exhancache.S,v
Working file: verify/toplevel/exhancache.S
head: 35.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 35.1
date: 1995/04/06 18:10:33;  author: jeffm;  state: Exp;
Test cached event handler and bbacking to cached code streams.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/gtlbaccess2.S,v
Working file: verify/toplevel/gtlbaccess2.S
head: 7.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 7.15
date: 1995/04/06 19:02:30;  author: jeffm;  state: Exp;  lines: +29 -7
Needed to add gtlb entry for dram (printing).
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/gtlbaccess3.S,v
Working file: verify/toplevel/gtlbaccess3.S
head: 7.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 1
description:
----------------------------
revision 7.14
date: 1995/04/06 19:02:32;  author: jeffm;  state: Exp;  lines: +18 -28
Needed to add gtlb entry for dram (printing).
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/gtlbaccess4.S,v
Working file: verify/toplevel/gtlbaccess4.S
head: 26.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
```

```
revision 26.4
date: 1995/04/06 19:02:34;  author: jeffm;  state: Exp;  lines: +22 -31
Needed to add gtlb entry for dram (printing).
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/gtlbmisseasy.S,v
Working file: verify/toplevel/gtlbmisseasy.S
head: 7.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 1
description:
----------------------------
revision 7.13
date: 1995/04/06 19:06:29;  author: jeffm;  state: Exp;  lines: +21 -6
Added gtlb entry for printing.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes_I1.S,v
Working file: verify/toplevel/hermes_I1.S
head: 35.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 35.1
date: 1995/04/04 01:20:36;  author: lisar;  state: Exp;
Interleave tests
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes_I2.S,v
Working file: verify/toplevel/hermes_I2.S
head: 35.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 35.1
date: 1995/04/04 01:20:39;  author: lisar;  state: Exp;
Interleave tests
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes_I4.S,v
Working file: verify/toplevel/hermes_I4.S
head: 35.2
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 35.1
date: 1995/04/04 01:20:41;  author: lisar;  state: Exp;
Interleave tests
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes_I_store_unique.S,v
Working file: verify/toplevel/hermes_I_store_unique.S
head: 35.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 35.1
date: 1995/04/04 01:20:44;  author: lisar;  state: Exp;
Interleave tests
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermeseasy_I1M0.S,v
Working file: verify/toplevel/hermeseasy_I1M0.S
head: 35.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 35.1
date: 1995/04/04 01:20:47;  author: lisar;  state: Exp;
Interleave tests
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/icache4k.S,v
Working file: verify/toplevel/icache4k.S
head: 33.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 33.2
date: 1995/04/03 16:30:34;  author: jeffm;  state: Exp;  lines: +5 -4
Fix out of range immediate values.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/template,v
Working file: verify/toplevel/template
head: 1.148
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 148;   selected revisions: 1
description:
----------------------------
revision 1.83
date: 1995/04/04 01:22:53;  author: lisar;  state: Exp;  lines: +68 -34
Periodic checkin.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/BOM,v
Working file: verilog/BOM
head: 6.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1390;  selected revisions: 13
description:
top level verilog BOM
----------------------------
revision 3.455
date: 1995/04/06 23:00:03;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc


Picked up placement BOMs and bug fixes as described below.
Have run 5woody in verilog simulation.


RCS file: /p/cvsroot/euterpe/verilog/bsrc/euterpe.V,v
revision 6.392
date: 1995/04/06 14:54:55 LT;  author: billz;  state: Exp;  lines: +4 -2
Added interface signal hz10or12back (HZ-something-or-other) to
cc.  Consistant with cc v1.77.

----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/uu/uuprblmr9.Veqn,v
RCS file: /p/cvsroot/euterpe/verilog/bsrc/uu/uu.V,v

revision 61.15
date: 1995/04/05 13:35:16 LT;  author: mws;  state: Exp;  lines: +13 -9
uu/uuprblmr9 uu/uu.V:  uuYieldsNbInR10 was on for Ifetch loopbacks, allowing
  CC to make new fill requests to NB and thus discarding loopbacks in progress.
  Test cachenasty3 accidentally noticed on a SN128WrtI.

----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/uu/uursrvduv.pla,v
revision 170.2
date: 1995/04/06 12:37:12 LT;  author: mws;  state: Exp;  lines: +2 -2
Unclosed comment lost EDepI/EWithdrawI check for both
  immediates > 31.  Found by veena test uu/edepi.pl.

----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/cc/ccseq.Veqn,v
revision 28.19
```

```
date: 1995/04/06 11:22:53 LT;  author: billz;  state: Exp;  lines: +2 -2
Corrected arc to oblivion in ccseq.Veqn.  Saved one atom.
----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/cc/cc.V,v
RCS file: /p/cvsroot/euterpe/verilog/bsrc/cc/cclatedirty.Veqn,v

revision 1.77
date: 1995/04/06 14:29:13 LT;  author: billz;  state: Exp;  lines: +24 -5
Adds the "cache index match 12 back" case to be a latedirty
case.  That is if a clean miss occurs and there happened to
be a store to the same cache line 12 cycles back, it turns
into a dirty miss, and the cache line is written back.

Caution: cc interface changes.  hz10or12backR5R6 signal added.

Haven't update placement yet; add the moment, need a gplace license.
Haven't updated euterpe yet, but will.

This problem brought to light in cachenasty2.
----------------------------------------
----------------------------
revision 3.454
date: 1995/04/06 21:55:37;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

change shape of placement - holein bottom right corner
----------------------------
revision 3.453
date: 1995/04/06 06:45:35;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc

move placement right and redo center control stipe to solve un-routes
----------------------------
revision 3.452
date: 1995/04/06 06:40:25;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

elliminate placement collisions
----------------------------
revision 3.451
date: 1995/04/06 06:37:15;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/es

move horizontal squeezing
----------------------------
revision 3.450
date: 1995/04/06 01:09:17;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cc

Check in of new placement.  58 rows. Aligned to
nb, at, and sr.  Converges in 0 iterations.

Note: this placement is generated from pimlib.pl.
And includes pla.pim and cc_misc.pim files.
----------------------------
revision 3.449
date: 1995/04/04 18:51:35;  author: tbr;  state: Exp;  lines: +2 -2
```

```
Release Target: euterpe/verilog/bsrc/hc

100% handplace hc1
----------------------------
revision 3.448
date: 1995/04/04 05:13:48;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

move control to center - saves 400 atoms
----------------------------
revision 3.447
date: 1995/04/04 00:27:47;  author: geert;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cp

New placement. Made space for VDDTS

Geert
----------------------------
revision 3.446
date: 1995/04/03 20:14:55;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

moved pc to bit positions 63:0 from 127:64 and moved bypass mux elements to free
up more horizontal tracks
----------------------------
revision 3.445
date: 1995/04/03 17:43:52;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gf

moved to align with bit positions 127:64 instead of 63:0
----------------------------
revision 3.444
date: 1995/04/03 07:16:02;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

uu/uursrvduu.tdcd cj/Makefile:
  Typo's left out GShuffleI4Mux (ex15test_0) and merge deposits
  (exresemdepitest1_0 and exresgmdepitest1_0).   Add rsrvdgsffli4mx.tst rule.
yy/tas.pl:  Typo's prevented shufflei4mux from being recognized.
----------------------------
revision 3.443
date: 1995/04/02 02:55:05;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

uu/uursrvduu.tdcd cj/rsrvd.tst Makefile:
  Typo left GCompressI out of the care sets and it then tended to become a
  reserved instruction (noticed by test xlu_subset_r1_1).
  Typo left GShuffleI and GShuffleI4Mux not checking their immediates (noticed
  by test ex15test_0).  Add rsrvdgshffli.tst rule.
tst/drvchk.V ife/ifetst.tst cj/cjrst.tst:
  Compatible with recent mem mngmnt pipelining.
tst/job.tst:  Comment out perl debug warnings.
ife/iffree.tst:  Experiments preparing for change in reset vector.
euterpe.status:
  Add note on LTLB changing under IFetch violating protection at new GVA.
  Remove note about lack of pipelined memory management enable.
  Add note on writeback reject bug worries.
```

```
  Add note on ICache size change exposure with mem management mode change.
Makefile euterpe_wrap.V i_euterpe_wrap.tb i_euterpe_wrap.vhdl:  lisar stuff.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/BOM,v
Working file: verilog/bsrc/BOM
head: 346.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1737;  selected revisions: 16
description:
----------------------------
revision 273.0
date: 1995/04/06 22:59:41;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Picked up placement BOMs and bug fixes as described below.
Have run 5woody in verilog simulation.


RCS file: /p/cvsroot/euterpe/verilog/bsrc/euterpe.V,v
revision 6.392
date: 1995/04/06 14:54:55 LT;  author: billz;  state: Exp;  lines: +4 -2
Added interface signal hz10or12back (HZ-something-or-other) to
cc.  Consistant with cc v1.77.

----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/uu/uuprblmr9.Veqn,v
RCS file: /p/cvsroot/euterpe/verilog/bsrc/uu/uu.V,v

revision 61.15
date: 1995/04/05 13:35:16 LT;  author: mws;  state: Exp;  lines: +13 -9
uu/uuprblmr9 uu/uu.V:  uuYieldsNbInR10 was on for Ifetch loopbacks, allowing
  CC to make new fill requests to NB and thus discarding loopbacks in progress.
  Test cachenasty3 accidentally noticed on a SN128WrtI.

----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/uu/uursrvduv.pla,v
revision 170.2
date: 1995/04/06 12:37:12 LT;  author: mws;  state: Exp;  lines: +2 -2
Unclosed comment lost EDepI/EWithdrawI check for both
  immediates > 31.  Found by veena test uu/edepi.pl.

----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/cc/ccseq.Veqn,v
revision 28.19
date: 1995/04/06 11:22:53 LT;  author: billz;  state: Exp;  lines: +2 -2
Corrected arc to oblivion in ccseq.Veqn.  Saved one atom.
----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/cc/cc.V,v
RCS file: /p/cvsroot/euterpe/verilog/bsrc/cc/cclatedirty.Veqn,v

revision 1.77
date: 1995/04/06 14:29:13 LT;  author: billz;  state: Exp;  lines: +24 -5
```

```
Adds the "cache index match 12 back" case to be a latedirty
case.  That is if a clean miss occurs and there happened to
be a store to the same cache line 12 cycles back, it turns
into a dirty miss, and the cache line is written back.

Caution: cc interface changes.  hz10or12backR5R6 signal added.

Haven't update placement yet; add the moment, need a gplace license.
Haven't updated euterpe yet, but will.

This problem brought to light in cachenasty2.
----------------------------------------
----------------------------
revision 272.11
date: 1995/04/06 22:59:26;  author: lisar;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 272.10
date: 1995/04/06 21:55:22;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

change shape of placement - holein bottom right corner
----------------------------
revision 272.9
date: 1995/04/06 06:45:19;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc

move placement right and redo center control stipe to solve un-routes
----------------------------
revision 272.8
date: 1995/04/06 06:40:10;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

elliminate placement collisions
----------------------------
revision 272.7
date: 1995/04/06 06:37:01;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/es

move horizontal squeezing
----------------------------
revision 272.6
date: 1995/04/06 01:08:55;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cc

Check in of new placement.  58 rows. Aligned to
nb, at, and sr.  Converges in 0 iterations.

Note: this placement is generated from pimlib.pl.
And includes pla.pim and cc_misc.pim files.
----------------------------
revision 272.5
date: 1995/04/04 18:51:15;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

100% handplace hc1
----------------------------
```

```
revision 272.4
date: 1995/04/04 05:13:33;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

move control to center - saves 400 atoms
----------------------------
revision 272.3
date: 1995/04/04 00:27:32;  author: geert;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cp

New placement. Made space for VDDTS

Geert
----------------------------
revision 272.2
date: 1995/04/03 20:14:41;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

moved pc to bit positions 63:0 from 127:64 and moved bypass mux elements to free
up more horizontal tracks
----------------------------
revision 272.1
date: 1995/04/03 17:43:34;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gf

moved to align with bit positions 127:64 instead of 63:0
----------------------------
revision 272.0
date: 1995/04/03 07:15:46;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uursrvduu.tdcd cj/Makefile:
  Typo's left out GShuffleI4Mux (ex15test_0) and merge deposits
  (exresemdepitest1_0 and exresgmdepitest1_0).   Add rsrvdgsffli4mx.tst rule.
yy/tas.pl:  Typo's prevented shufflei4mux from being recognized.
----------------------------
revision 271.1
date: 1995/04/03 07:15:35;  author: mws;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 271.0
date: 1995/04/02 02:54:40;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uursrvduu.tdcd cj/rsrvd.tst Makefile:
  Typo left GCompressI out of the care sets and it then tended to become a
  reserved instruction (noticed by test xlu_subset_r1_1).
  Typo left GShuffleI and GShuffleI4Mux not checking their immediates (noticed
  by test ex15test_0).  Add rsrvdgshffli.tst rule.
tst/drvchk.V ife/ifetst.tst cj/cjrst.tst:
  Compatible with recent mem mngmnt pipelining.
tst/job.tst:  Comment out perl debug warnings.
ife/iffree.tst:  Experiments preparing for change in reset vector.
euterpe.status:
  Add note on LTLB changing under IFetch violating protection at new GVA.
  Remove note about lack of pipelined memory management enable.
  Add note on writeback reject bug worries.
```

```
  Add note on ICache size change exposure with mem management mode change.
Makefile euterpe_wrap.V i_euterpe_wrap.tb i_euterpe_wrap.vhdl:  lisar stuff.
----------------------------
revision 270.3
date: 1995/04/02 02:54:20;  author: mws;  state: Exp;  lines: +10 -10
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/analog_euterpe.hwc,v
Working file: verilog/bsrc/analog_euterpe.hwc
head: 35.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 35.5
date: 1995/04/03 23:44:37;  author: geert;  state: Exp;  lines: +2 -4
Changed obstruction mask for VDDTS
Geert
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.V,v
Working file: verilog/bsrc/euterpe.V
head: 6.431
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 431;   selected revisions: 2
description:
----------------------------
revision 6.392
date: 1995/04/06 21:54:55;  author: billz;  state: Exp;  lines: +4 -2
Added interface signal hz10or12back (HZ-something-or-other) to
cc.  Consistant with cc v1.77.
----------------------------
revision 6.391
date: 1995/04/03 17:40:44;  author: dickson;  state: Exp;  lines: +2 -2
changed operand hookup to gf from bits 63:0 to 127:64
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.status,v
Working file: verilog/bsrc/euterpe.status
head: 24.83
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 83;    selected revisions: 2
description:
----------------------------
revision 24.50
date: 1995/04/05 20:38:44;  author: mws;  state: Exp;  lines: +25 -1
One serious bug & lots of silly logic.
```

```
----------------------------
revision 24.49
date: 1995/04/02 02:23:25;  author: mws;  state: Exp;  lines: +9 -1
  Add note on LTLB changing under IFetch violating protection at new GVA.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/i_euterpe_wrap.tb,v
Working file: verilog/bsrc/i_euterpe_wrap.tb
head: 187.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 187.8
date: 1995/04/06 21:16:21;  author: lisar;  state: Exp;  lines: +1 -10
Don't instantiate snoop yet
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/BOM,v
Working file: verilog/bsrc/cc/BOM
head: 92.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 182;   selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 75.0
date: 1995/04/06 22:53:24;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Picked up placement BOMs and bug fixes as described below.
Have run 5woody in verilog simulation.


RCS file: /p/cvsroot/euterpe/verilog/bsrc/euterpe.V,v
revision 6.392
date: 1995/04/06 14:54:55 LT;  author: billz;  state: Exp;  lines: +4 -2
Added interface signal hz10or12back (HZ-something-or-other) to
cc.  Consistant with cc v1.77.

----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/uu/uuprblmr9.Veqn,v
RCS file: /p/cvsroot/euterpe/verilog/bsrc/uu/uu.V,v

revision 61.15
date: 1995/04/05 13:35:16 LT;  author: mws;  state: Exp;  lines: +13 -9
uu/uuprblmr9 uu/uu.V:  uuYieldsNbInR10 was on for Ifetch loopbacks, allowing
  CC to make new fill requests to NB and thus discarding loopbacks in progress.
  Test cachenasty3 accidentally noticed on a SN128WrtI.
```

```
----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/uu/uursrvduv.pla,v
revision 170.2
date: 1995/04/06 12:37:12 LT;  author: mws;  state: Exp;  lines: +2 -2
Unclosed comment lost EDepI/EWithdrawI check for both
  immediates > 31.  Found by veena test uu/edepi.pl.

----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/cc/ccseq.Veqn,v
revision 28.19
date: 1995/04/06 11:22:53 LT;  author: billz;  state: Exp;  lines: +2 -2
Corrected arc to oblivion in ccseq.Veqn.  Saved one atom.
----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/cc/cc.V,v
RCS file: /p/cvsroot/euterpe/verilog/bsrc/cc/cclatedirty.Veqn,v

revision 1.77
date: 1995/04/06 14:29:13 LT;  author: billz;  state: Exp;  lines: +24 -5
Adds the "cache index match 12 back" case to be a latedirty
case.  That is if a clean miss occurs and there happened to
be a store to the same cache line 12 cycles back, it turns
into a dirty miss, and the cache line is written back.

Caution: cc interface changes.  hz10or12backR5R6 signal added.

Haven't update placement yet; add the moment, need a gplace license.
Haven't updated euterpe yet, but will.

This problem brought to light in cachenasty2.
----------------------------------------
----------------------------
revision 74.1
date: 1995/04/06 22:53:17;  author: lisar;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 74.0
date: 1995/04/06 01:08:18;  author: billz;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/cc

Check in of new placement.  58 rows. Aligned to
nb, at, and sr.  Converges in 0 iterations.

Note: this placement is generated from pimlib.pl.
And includes pla.pim and cc_misc.pim files.
----------------------------
revision 73.1
date: 1995/04/06 01:08:10;  author: billz;  state: Exp;  lines: +13 -12
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/Makefile,v
Working file: verilog/bsrc/cc/Makefile
head: 1.27
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 27;    selected revisions: 2
description:
----------------------------
revision 1.23
date: 1995/04/06 23:12:27;  author: billz;  state: Exp;  lines: +1 -3
Placement is updated.
Changes to cc.V: just declared wire busy.
Makefile: just changed GARDS_DISPLAY.
----------------------------
revision 1.22
date: 1995/04/06 01:05:25;  author: billz;  state: Exp;  lines: +2 -2
Check in of new placement.  58 rows. Aligned to
nb, at, and sr.  Converges in 0 iterations.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cc.V,v
Working file: verilog/bsrc/cc/cc.V
head: 1.87
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 87;    selected revisions: 3
description:
----------------------------
revision 1.78
date: 1995/04/06 23:12:31;  author: billz;  state: Exp;  lines: +2 -2
Placement is updated.
Changes to cc.V: just declared wire busy.
Makefile: just changed GARDS_DISPLAY.
----------------------------
revision 1.77
date: 1995/04/06 21:29:13;  author: billz;  state: Exp;  lines: +24 -5
Adds the "cache index match 12 back" case to be a latedirty
case.  That is if a clean miss occurs and there happened to
be a store to the same cache line 12 cycles back, it turns
into a dirty miss, and the cache line is written back.

Caution: cc interface changes.  hz10or12backR5R6 signal added.

Haven't update placement yet; add the moment, need a gplace license.
Haven't updated euterpe yet, but will.

This problem brought to light in cachenasty2.
----------------------------
revision 1.76
date: 1995/04/06 01:05:28;  author: billz;  state: Exp;  lines: +5 -4
Check in of new placement.  58 rows. Aligned to
nb, at, and sr.  Converges in 0 iterations.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cc_misc.pim,v
Working file: verilog/bsrc/cc/cc_misc.pim
head: 73.3
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 73.1
date: 1995/04/06 01:05:30;  author: billz;  state: Exp;
Check in of new placement.  58 rows. Aligned to
nb, at, and sr.  Converges in 0 iterations.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cccount.pla,v
Working file: verilog/bsrc/cc/cccount.pla
head: 28.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 1
description:
----------------------------
revision 28.6
date: 1995/04/06 01:05:32;  author: billz;  state: Exp;  lines: +2 -1
Check in of new placement.  58 rows. Aligned to
nb, at, and sr.  Converges in 0 iterations.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cchexcount.pla,v
Working file: verilog/bsrc/cc/cchexcount.pla
head: 28.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 1
description:
----------------------------
revision 28.5
date: 1995/04/06 01:05:34;  author: billz;  state: Exp;  lines: +2 -1
Check in of new placement.  58 rows. Aligned to
nb, at, and sr.  Converges in 0 iterations.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cchold.Veqn,v
Working file: verilog/bsrc/cc/cchold.Veqn
head: 60.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 60.3
date: 1995/04/06 01:05:36;  author: billz;  state: Exp;  lines: +2 -1
Check in of new placement.  58 rows. Aligned to
nb, at, and sr.  Converges in 0 iterations.
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cclatedirty.Veqn,v
Working file: verilog/bsrc/cc/cclatedirty.Veqn
head: 40.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 2
description:
----------------------------
revision 40.7
date: 1995/04/06 21:29:15;  author: billz;  state: Exp;  lines: +7 -5
Adds the "cache index match 12 back" case to be a latedirty
case.  That is if a clean miss occurs and there happened to
be a store to the same cache line 12 cycles back, it turns
into a dirty miss, and the cache line is written back.

Caution: cc interface changes.  hz10or12backR5R6 signal added.

Haven't update placement yet; add the moment, need a gplace license.
Haven't updated euterpe yet, but will.

This problem brought to light in cachenasty2.
----------------------------
revision 40.6
date: 1995/04/06 01:05:37;  author: billz;  state: Exp;  lines: +2 -1
Check in of new placement.  58 rows. Aligned to
nb, at, and sr.  Converges in 0 iterations.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/ccrcv.Veqn,v
Working file: verilog/bsrc/cc/ccrcv.Veqn
head: 51.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
----------------------------
revision 51.6
date: 1995/04/06 01:05:39;  author: billz;  state: Exp;  lines: +2 -1
Check in of new placement.  58 rows. Aligned to
nb, at, and sr.  Converges in 0 iterations.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/ccseq.Veqn,v
Working file: verilog/bsrc/cc/ccseq.Veqn
head: 28.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 2
description:
----------------------------
```

```
revision 28.19
date: 1995/04/06 18:22:53;  author: billz;  state: Exp;  lines: +2 -2
Corrected arc to oblivion in ccseq.Veqn.  Saved one atom.
----------------------------
revision 28.18
date: 1995/04/06 01:05:40;  author: billz;  state: Exp;  lines: +2 -1
Check in of new placement.  58 rows. Aligned to
nb, at, and sr.  Converges in 0 iterations.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/ccstart.Veqn,v
Working file: verilog/bsrc/cc/ccstart.Veqn
head: 24.18
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 18;    selected revisions: 1
description:
----------------------------
revision 24.16
date: 1995/04/06 01:05:42;  author: billz;  state: Exp;  lines: +2 -2
Check in of new placement.  58 rows. Aligned to
nb, at, and sr.  Converges in 0 iterations.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cctester.V,v
Working file: verilog/bsrc/cc/cctester.V
head: 1.21
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 21;    selected revisions: 1
description:
----------------------------
revision 1.21
date: 1995/04/06 21:29:16;  author: billz;  state: Exp;  lines: +5 -2
Adds the "cache index match 12 back" case to be a latedirty
case.  That is if a clean miss occurs and there happened to
be a store to the same cache line 12 cycles back, it turns
into a dirty miss, and the cache line is written back.

Caution: cc interface changes.  hz10or12backR5R6 signal added.

Haven't update placement yet; add the moment, need a gplace license.
Haven't updated euterpe yet, but will.

This problem brought to light in cachenasty2.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/genpim.pl,v
Working file: verilog/bsrc/cc/genpim.pl
head: 5.20
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 20;    selected revisions: 1
description:
----------------------------
revision 5.14
date: 1995/04/06 01:05:44;  author: billz;  state: Exp;  lines: +2 -3
Check in of new placement.  58 rows. Aligned to
nb, at, and sr.  Converges in 0 iterations.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/pimlib.pl,v
Working file: verilog/bsrc/cc/pimlib.pl
head: 5.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16;    selected revisions: 2
description:
----------------------------
revision 5.14
date: 1995/04/06 23:12:33;  author: billz;  state: Exp;  lines: +3 -2
Placement is updated.
Changes to cc.V: just declared wire busy.
Makefile: just changed GARDS_DISPLAY.
----------------------------
revision 5.13
date: 1995/04/06 01:05:46;  author: billz;  state: Exp;  lines: +114 -2
Check in of new placement.  58 rows. Aligned to
nb, at, and sr.  Converges in 0 iterations.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cdio/cdio.V,v
Working file: verilog/bsrc/cdio/cdio.V
head: 1.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 1
description:
----------------------------
revision 1.19
date: 1995/04/06 23:36:57;  author: billz;  state: Exp;  lines: +9 -9
An attempt to fix the "dinX5X8[127:64] hold for 2 cycles, not 4" problem.
What happened to cdio_tester.V?  I'd be useful.  I've got a
cdio_tester.v, but see no cdio_tester.V in cvs.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/ceregcore.V,v
Working file: verilog/bsrc/ce/ceregcore.V
head: 1.44
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 44;    selected revisions: 1
```

```
description:
----------------------------
revision 1.34
date: 1995/04/05 06:10:06;  author: dickson;  state: Exp;  lines: +14 -7
added force of hchdis_abm and dhchdis_abm after machine check
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/BOM,v
Working file: verilog/bsrc/cj/BOM
head: 122.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 259;   selected revisions: 4
description:
----------------------------
revision 109.0
date: 1995/04/03 07:04:03;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uursrvduu.tdcd cj/Makefile:
  Typo's left out GShuffleI4Mux (ex15test_0) and merge deposits
  (exresemdepitest1_0 and exresgmdepitest1_0).   Add rsrvdgsffli4mx.tst rule.
----------------------------
revision 108.1
date: 1995/04/03 07:03:56;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 108.0
date: 1995/04/02 02:46:44;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uursrvduu.tdcd cj/rsrvd.tst Makefile:
  Typo left GCompressI out of the care sets and it then tended to become a
  reserved instruction (noticed by test xlu_subset_r1_1).
  Typo left GShuffleI and GShuffleI4Mux not checking their immediates (noticed
  by test ex15test_0).  Add rsrvdgshffli.tst rule.
tst/drvchk.V ife/ifetst.tst cj/cjrst.tst:
  Compatible with recent mem mngmnt pipelining.
tst/job.tst:  Comment out perl debug warnings.
ife/iffree.tst:  Experiments preparing for change in reset vector.
euterpe.status:
  Add note on LTLB changing under IFetch violating protection at new GVA.
  Remove note about lack of pipelined memory management enable.
  Add note on writeback reject bug worries.
  Add note on ICache size change exposure with mem management mode change.
Makefile euterpe_wrap.V i_euterpe_wrap.tb i_euterpe_wrap.vhdl:  lisar stuff.
----------------------------
revision 107.1
date: 1995/04/02 02:46:35;  author: mws;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/Makefile,v
Working file: verilog/bsrc/cj/Makefile
head: 1.41
```

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 41;    selected revisions: 3
description:
----------------------------
revision 1.40
date: 1995/04/06 18:24:36;  author: mws;  state: Exp;  lines: +5 -1
Add rsrvdedepi.tst rule.
----------------------------
revision 1.39
date: 1995/04/03 07:02:34;  author: mws;  state: Exp;  lines: +6 -2
uu/uursrvduu.tdcd cj/Makefile:
  Typo's left out GShuffleI4Mux (ex15test_0) and merge deposits
  (exresemdepitest1_0 and exresgmdepitest1_0).   Add rsrvdgsffli4mx.tst rule.
----------------------------
revision 1.38
date: 1995/04/02 02:20:34;  author: mws;  state: Exp;  lines: +8 -3
uu/uursrvduu.tdcd cj/rsrvd.tst Makefile:
  Typo left GCompressI out of the care sets and it then tended to become a
  reserved instruction (noticed by test xlu_subset_r1_1).
  Typo left GShuffleI and GShuffleI4Mux not checking their immediates (noticed
  by test ex15test_0).  Add rsrvdgshffli.tst rule.
tst/drvchk.V ife/ifetst.tst cj/cjrst.tst:
  Compatible with recent mem mngmnt pipelining.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/cjrst.tst,v
Working file: verilog/bsrc/cj/cjrst.tst
head: 13.39
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 39;    selected revisions: 1
description:
----------------------------
revision 13.33
date: 1995/04/02 02:20:36;  author: mws;  state: Exp;  lines: +3 -3
uu/uursrvduu.tdcd cj/rsrvd.tst Makefile:
  Typo left GCompressI out of the care sets and it then tended to become a
  reserved instruction (noticed by test xlu_subset_r1_1).
  Typo left GShuffleI and GShuffleI4Mux not checking their immediates (noticed
  by test ex15test_0).  Add rsrvdgshffli.tst rule.
tst/drvchk.V ife/ifetst.tst cj/cjrst.tst:
  Compatible with recent mem mngmnt pipelining.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/rsrvd.tst,v
Working file: verilog/bsrc/cj/rsrvd.tst
head: 78.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 1
```

```
description:
----------------------------
revision 78.8
date: 1995/04/02 02:20:37;  author: mws;  state: Exp;  lines: +13 -14
uu/uursrvduu.tdcd cj/rsrvd.tst Makefile:
  Typo left GCompressI out of the care sets and it then tended to become a
  reserved instruction (noticed by test xlu_subset_r1_1).
  Typo left GShuffleI and GShuffleI4Mux not checking their immediates (noticed
  by test ex15test_0).  Add rsrvdgshffli.tst rule.
tst/drvchk.V ife/ifetst.tst cj/cjrst.tst:
  Compatible with recent mem mngmnt pipelining.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/BOM,v
Working file: verilog/bsrc/cp/BOM
head: 60.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 119;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 48.0
date: 1995/04/04 00:27:14;  author: geert;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/cp

New placement. Made space for VDDTS

Geert
----------------------------
revision 47.1
date: 1995/04/04 00:27:06;  author: geert;  state: Exp;  lines: +7 -6
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/clean-request,v
Working file: verilog/bsrc/cp/clean-request
head: 9.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
revision 9.8
date: 1995/04/04 00:25:50;  author: geert;  state: Exp;  lines: +2 -1
Made some space for the vddts wire

Geert
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/cph.pim,v
Working file: verilog/bsrc/cp/cph.pim
head: 41.8
```

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 41.5
date: 1995/04/04 00:25:55;  author: geert;  state: Exp;  lines: +0 -238
Made some space for the vddts wire

Geert
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/cphh.pim,v
Working file: verilog/bsrc/cp/cphh.pim
head: 47.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 47.1
date: 1995/04/04 00:25:57;  author: geert;  state: Exp;
Made some space for the vddts wire

Geert
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/genpim.pl,v
Working file: verilog/bsrc/cp/genpim.pl
head: 5.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 5.10
date: 1995/04/04 00:26:04;  author: geert;  state: Exp;  lines: +8 -1
Made some space for the vddts wire

Geert
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/pimlib.pl,v
Working file: verilog/bsrc/cp/pimlib.pl
head: 5.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
```

```
----------------------------
revision 5.4
date: 1995/04/04 00:26:06;  author: geert;  state: Exp;  lines: +8 -1
Made some space for the vddts wire

Geert
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/BOM,v
Working file: verilog/bsrc/es/BOM
head: 97.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 198;   selected revisions: 2
description:
----------------------------
revision 84.0
date: 1995/04/06 06:36:44;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/es

move horizontal squeezing
----------------------------
revision 83.1
date: 1995/04/06 06:36:37;  author: dickson;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/clean-request,v
Working file: verilog/bsrc/es/clean-request
head: 45.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 45.13
date: 1995/04/06 06:35:43;  author: dickson;  state: Exp;  lines: +2 -1
start clean on next releasebom
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/es.pim,v
Working file: verilog/bsrc/es/es.pim
head: 5.55
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 55;    selected revisions: 1
description:
----------------------------
revision 5.47
date: 1995/04/06 06:34:58;  author: dickson;  state: Exp;  lines: +6447 -6447
more horizontal squeezing
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gf/BOM,v
Working file: verilog/bsrc/gf/BOM
head: 37.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 72;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 30.0
date: 1995/04/03 17:43:16;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/gf

moved to align with bit positions 127:64 instead of 63:0
----------------------------
revision 29.1
date: 1995/04/03 17:43:08;  author: dickson;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gf/gf.pim,v
Working file: verilog/bsrc/gf/gf.pim
head: 4.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 4.10
date: 1995/04/03 17:42:08;  author: dickson;  state: Exp;  lines: +8 -32
moved placement to aligne with bit positions 127:64 instead
of 63:0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/BOM,v
Working file: verilog/bsrc/gt/BOM
head: 98.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 194;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 81.0
date: 1995/04/04 05:13:16;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/gt

move control to center - saves 400 atoms
----------------------------
```

```
revision 80.1
date: 1995/04/04 05:13:09;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/pimlib.pl,v
Working file: verilog/bsrc/gt/pimlib.pl
head: 26.23
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 23;    selected revisions: 1
description:
----------------------------
revision 26.14
date: 1995/04/04 05:12:32;  author: tbr;  state: Exp;  lines: +50 -45
move control to center - saves 400 atoms
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/BOM,v
Working file: verilog/bsrc/hc/BOM
head: 125.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 250;   selected revisions: 6
description:
releasebom adding BOM
----------------------------
revision 101.0
date: 1995/04/06 21:55:05;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/hc

change shape of placement - holein bottom right corner
----------------------------
revision 100.1
date: 1995/04/06 21:54:58;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 100.0
date: 1995/04/06 21:53:51;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/hc

change shape of placement - holein bottom right corner
----------------------------
revision 99.1
date: 1995/04/06 21:53:44;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 99.0
date: 1995/04/04 18:50:55;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/hc

100% handplace hc1
----------------------------
```

```
revision 98.1
date: 1995/04/04 18:50:47;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc.V,v
Working file: verilog/bsrc/hc/hc.V
head: 1.56
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 56;    selected revisions: 2
description:
----------------------------
revision 1.52
date: 1995/04/04 19:58:12;  author: woody;  state: Exp;  lines: +2 -4
Added missing pins to mnemo body.
Added isolation circuit to the mnemo pll reference voltage.
Added gnd to connector.
----------------------------
revision 1.51
date: 1995/04/04 16:27:08;  author: woody;  state: Exp;  lines: +2 -4
hc was forcing event daemon stores to be blocking by forcing the low order bits
of the address to indicate octlet 1. HC will no longer do this forcing. It is
the responsibility of the SW to use an address that will block.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/pimlib.pl,v
Working file: verilog/bsrc/hc/pimlib.pl
head: 27.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 3
description:
----------------------------
revision 27.8
date: 1995/04/06 21:53:11;  author: tbr;  state: Exp;  lines: +11 -9
change shape of placement - holein bottom right corner
----------------------------
revision 27.7
date: 1995/04/04 19:58:15;  author: woody;  state: Exp;  lines: +1 -3
Added missing pins to mnemo body.
Added isolation circuit to the mnemo pll reference voltage.
Added gnd to connector.
----------------------------
revision 27.6
date: 1995/04/04 18:48:52;  author: tbr;  state: Exp;  lines: +277 -4
100% handplace hc1
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/BOM,v
Working file: verilog/bsrc/ife/BOM
head: 68.1
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 140;   selected revisions: 2
description:
----------------------------
revision 59.0
date: 1995/04/02 02:49:46;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uursrvduu.tdcd cj/rsrvd.tst Makefile:
  Typo left GCompressI out of the care sets and it then tended to become a
  reserved instruction (noticed by test xlu_subset_r1_1).
  Typo left GShuffleI and GShuffleI4Mux not checking their immediates (noticed
  by test ex15test_0).  Add rsrvdgshffli.tst rule.
tst/drvchk.V ife/ifetst.tst cj/cjrst.tst:
  Compatible with recent mem mngmnt pipelining.
tst/job.tst:  Comment out perl debug warnings.
ife/iffree.tst:  Experiments preparing for change in reset vector.
euterpe.status:
  Add note on LTLB changing under IFetch violating protection at new GVA.
  Remove note about lack of pipelined memory management enable.
  Add note on writeback reject bug worries.
  Add note on ICache size change exposure with mem management mode change.
Makefile euterpe_wrap.V i_euterpe_wrap.tb i_euterpe_wrap.vhdl:  lisar stuff.
----------------------------
revision 58.1
date: 1995/04/02 02:49:36;  author: mws;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/iffree.tst,v
Working file: verilog/bsrc/ife/iffree.tst
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 1.5
date: 1995/04/02 02:21:09;  author: mws;  state: Exp;  lines: +14 -10
tst/drvchk.V ife/ifetst.tst cj/cjrst.tst:
  Compatible with recent mem mngmnt pipelining.
ife/iffree.tst:  Experiments preparing for change in reset vector.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/ifrst.tst,v
Working file: verilog/bsrc/ife/ifrst.tst
head: 2.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
```

```
----------------------------
revision 2.9
date: 1995/04/02 02:21:11;  author: mws;  state: Exp;  lines: +2 -2
tst/drvchk.V ife/ifetst.tst cj/cjrst.tst:
  Compatible with recent mem mngmnt pipelining.
ife/iffree.tst:  Experiments preparing for change in reset vector.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/BOM,v
Working file: verilog/bsrc/mc/BOM
head: 79.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 157;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 66.0
date: 1995/04/06 06:45:02;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/mc

move placement right and redo center control stipe to solve un-routes
----------------------------
revision 65.1
date: 1995/04/06 06:44:54;  author: dickson;  state: Exp;  lines: +6 -6
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/clean-request,v
Working file: verilog/bsrc/mc/clean-request
head: 17.19
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 19;    selected revisions: 2
description:
----------------------------
revision 17.14
date: 1995/04/06 06:43:45;  author: dickson;  state: Exp;  lines: +2 -1
start clean on next releasebom
----------------------------
revision 17.13
date: 1995/04/06 06:41:15;  author: dickson;  state: Exp;  lines: +2 -1
move placement to right and redo center control stripe
to solve un-routes in this area
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/genpim.pl,v
Working file: verilog/bsrc/mc/genpim.pl
head: 13.17
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 17;    selected revisions: 1
description:
----------------------------
revision 13.12
date: 1995/04/06 06:41:17;  author: dickson;  state: Exp;  lines: +3 -3
move placement to right and redo center control stripe
to solve un-routes in this area
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/mc.control.pim,v
Working file: verilog/bsrc/mc/mc.control.pim
head: 48.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 48.6
date: 1995/04/06 06:41:19;  author: dickson;  state: Exp;  lines: +594 -754
move placement to right and redo center control stripe
to solve un-routes in this area
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/mc.dataHigh.pim,v
Working file: verilog/bsrc/mc/mc.dataHigh.pim
head: 48.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
revision 48.6
date: 1995/04/06 06:41:21;  author: dickson;  state: Exp;  lines: +1268 -1268
move placement to right and redo center control stripe
to solve un-routes in this area
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/mc.dataLow.pim,v
Working file: verilog/bsrc/mc/mc.dataLow.pim
head: 48.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 48.5
date: 1995/04/06 06:41:24;  author: dickson;  state: Exp;  lines: +1246 -1246
move placement to right and redo center control stripe
to solve un-routes in this area
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/BOM,v
Working file: verilog/bsrc/rg/BOM
head: 136.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 297;   selected revisions: 4
description:
----------------------------
revision 110.0
date: 1995/04/06 06:39:48;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/rg

elliminate placement collisions
----------------------------
revision 109.1
date: 1995/04/06 06:39:40;  author: dickson;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 109.0
date: 1995/04/03 20:14:26;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/rg

moved pc to bit positions 63:0 from 127:64 and moved bypass mux elements to free
up more horizontal tracks
----------------------------
revision 108.1
date: 1995/04/03 20:14:18;  author: dickson;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/clean-request,v
Working file: verilog/bsrc/rg/clean-request
head: 60.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 60.8
date: 1995/04/06 06:38:38;  author: dickson;  state: Exp;  lines: +1 -0
placement change to elliminate collisions in top level placement
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rg.pim,v
Working file: verilog/bsrc/rg/rg.pim
head: 82.31
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 31;    selected revisions: 2
description:
----------------------------
```

```
revision 82.16
date: 1995/04/06 06:38:41;  author: dickson;  state: Exp;  lines: +2622 -2622
placement change to elliminate collisions in top level placement
----------------------------
revision 82.15
date: 1995/04/03 19:57:02;  author: dickson;  state: Exp;  lines: +2629 -2629
moved pc blocks to align with bits 63:0 was 127:64
also moved muxes and mux f/f's of bypass mux in rg
in a different order to free up more horizontal tracks.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/BOM,v
Working file: verilog/bsrc/tst/BOM
head: 112.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 234;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 102.0
date: 1995/04/02 02:52:20;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uursrvduu.tdcd cj/rsrvd.tst Makefile:
  Typo left GCompressI out of the care sets and it then tended to become a
  reserved instruction (noticed by test xlu_subset_r1_1).
  Typo left GShuffleI and GShuffleI4Mux not checking their immediates (noticed
  by test ex15test_0).  Add rsrvdgshffli.tst rule.
tst/drvchk.V ife/ifetst.tst cj/cjrst.tst:
  Compatible with recent mem mngmnt pipelining.
tst/job.tst:  Comment out perl debug warnings.
ife/iffree.tst:  Experiments preparing for change in reset vector.
euterpe.status:
  Add note on LTLB changing under IFetch violating protection at new GVA.
  Remove note about lack of pipelined memory management enable.
  Add note on writeback reject bug worries.
  Add note on ICache size change exposure with mem management mode change.
Makefile euterpe_wrap.V i_euterpe_wrap.tb i_euterpe_wrap.vhdl:  lisar stuff.
----------------------------
revision 101.1
date: 1995/04/02 02:52:09;  author: mws;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/drvchk.V,v
Working file: verilog/bsrc/tst/drvchk.V
head: 1.85
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 85;    selected revisions: 1
description:
----------------------------
```

```
revision 1.77
date: 1995/04/02 02:06:35;  author: mws;  state: Exp;  lines: +3 -3
tst/drvchk.V:  Compatible with recent mem mngmnt pipelining.
tst/job.tst:  Comment out perl debug warnings.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/job.tst,v
Working file: verilog/bsrc/tst/job.tst
head: 6.41
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 41;    selected revisions: 1
description:
----------------------------
revision 6.36
date: 1995/04/02 02:06:38;  author: mws;  state: Exp;  lines: +3 -3
tst/drvchk.V:  Compatible with recent mem mngmnt pipelining.
tst/job.tst:  Comment out perl debug warnings.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/BOM,v
Working file: verilog/bsrc/uu/BOM
head: 218.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 480;   selected revisions: 6
description:
----------------------------
revision 175.0
date: 1995/04/06 22:58:15;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Picked up placement BOMs and bug fixes as described below.
Have run 5woody in verilog simulation.


RCS file: /p/cvsroot/euterpe/verilog/bsrc/euterpe.V,v
revision 6.392
date: 1995/04/06 14:54:55 LT;  author: billz;  state: Exp;  lines: +4 -2
Added interface signal hz10or12back (HZ-something-or-other) to
cc.  Consistant with cc v1.77.

----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/uu/uuprblmr9.Veqn,v
RCS file: /p/cvsroot/euterpe/verilog/bsrc/uu/uu.V,v

revision 61.15
date: 1995/04/05 13:35:16 LT;  author: mws;  state: Exp;  lines: +13 -9
uu/uuprblmr9 uu/uu.V:  uuYieldsNbInR10 was on for Ifetch loopbacks, allowing
  CC to make new fill requests to NB and thus discarding loopbacks in progress.
  Test cachenasty3 accidentally noticed on a SN128WrtI.
```

```
----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/uu/uursrvduv.pla,v
revision 170.2
date: 1995/04/06 12:37:12 LT;  author: mws;  state: Exp;  lines: +2 -2
Unclosed comment lost EDepI/EWithdrawI check for both
  immediates > 31.  Found by veena test uu/edepi.pl.

----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/cc/ccseq.Veqn,v
revision 28.19
date: 1995/04/06 11:22:53 LT;  author: billz;  state: Exp;  lines: +2 -2
Corrected arc to oblivion in ccseq.Veqn.  Saved one atom.
----------------------------
RCS file: /p/cvsroot/euterpe/verilog/bsrc/cc/cc.V,v
RCS file: /p/cvsroot/euterpe/verilog/bsrc/cc/cclatedirty.Veqn,v

revision 1.77
date: 1995/04/06 14:29:13 LT;  author: billz;  state: Exp;  lines: +24 -5
Adds the "cache index match 12 back" case to be a latedirty
case.  That is if a clean miss occurs and there happened to
be a store to the same cache line 12 cycles back, it turns
into a dirty miss, and the cache line is written back.

Caution: cc interface changes.  hz10or12backR5R6 signal added.

Haven't update placement yet; add the moment, need a gplace license.
Haven't updated euterpe yet, but will.

This problem brought to light in cachenasty2.
------------------------------------------
----------------------------
revision 174.1
date: 1995/04/06 22:58:06;  author: lisar;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 174.0
date: 1995/04/03 07:07:54;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uursrvduu.tdcd cj/Makefile:
  Typo's left out GShuffleI4Mux (ex15test_0) and merge deposits
  (exresemdepitest1_0 and exresgmdepitest1_0).   Add rsrvdgsffli4mx.tst rule.
----------------------------
revision 173.1
date: 1995/04/03 07:07:45;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 173.0
date: 1995/04/02 02:53:09;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uursrvduu.tdcd cj/rsrvd.tst Makefile:
  Typo left GCompressI out of the care sets and it then tended to become a
  reserved instruction (noticed by test xlu_subset_r1_1).
  Typo left GShuffleI and GShuffleI4Mux not checking their immediates (noticed
  by test ex15test_0).  Add rsrvdgshffli.tst rule.
tst/drvchk.V ife/ifetst.tst cj/cjrst.tst:
```

```
  Compatible with recent mem mngmnt pipelining.
tst/job.tst:  Comment out perl debug warnings.
ife/iffree.tst:  Experiments preparing for change in reset vector.
euterpe.status:
  Add note on LTLB changing under IFetch violating protection at new GVA.
  Remove note about lack of pipelined memory management enable.
  Add note on writeback reject bug worries.
  Add note on ICache size change exposure with mem management mode change.
Makefile euterpe_wrap.V i_euterpe_wrap.tb i_euterpe_wrap.vhdl:  lisar stuff.
----------------------------
revision 172.1
date: 1995/04/02 02:52:58;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/genpim.pl,v
Working file: verilog/bsrc/uu/genpim.pl
head: 68.17
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 17;    selected revisions: 1
description:
----------------------------
revision 68.14
date: 1995/04/03 14:19:54;  author: woody;  state: Exp;  lines: +2 -2
genpim.pl: remove '.noPifPack' to help toplevel placement.

pimplib.pl: more improvement on the mincut placement seed. This verision
contains >1/3 of uu. All of the bypass comparators and all of the Problem Code
Pipeline.

uu_control.pim: complete placement of uu/BOM 173.0. Trying to keep up.

success in pass3:

Atoms:                  count atom  bjt   isrc  pld   clock
       BJT Totals:      3785  25911 58156 41702 35960 17684


    Generating Gards Nets file gards/uu.slack
    Generating instance drive strength file gards/uu-pass3.strength
    Disgorging sdl file gards/uu-pass3.sdl
      Writing sdl structure: gards_47_uu_46_edif

      Congratulations!  No timing or DC Load violations!

Memory usage: 37.422MB
Exit code: 0 (Success)
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/pimlib.pl,v
Working file: verilog/bsrc/uu/pimlib.pl
head: 68.14
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 2
description:
----------------------------
revision 68.13
date: 1995/04/04 19:44:20;  author: woody;  state: Exp;  lines: +47 -8
Latest placement. Getting better, but still doesn't converge.
----------------------------
revision 68.12
date: 1995/04/03 14:19:56;  author: woody;  state: Exp;  lines: +430 -78
genpim.pl: remove '.noPifPack' to help toplevel placement.

pimplib.pl: more improvement on the mincut placement seed. This verision
contains >1/3 of uu. All of the bypass comparators and all of the Problem Code
Pipeline.

uu_control.pim: complete placement of uu/BOM 173.0. Trying to keep up.

success in pass3:

Atoms:                  count atom  bjt   isrc  pld   clock
       BJT Totals:      3785  25911 58156 41702 35960 17684


    Generating Gards Nets file gards/uu.slack
    Generating instance drive strength file gards/uu-pass3.strength
    Disgorging sdl file gards/uu-pass3.sdl
      Writing sdl structure: gards_47_uu_46_edif

      Congratulations!  No timing or DC Load violations!

Memory usage: 37.422MB
Exit code: 0 (Success)
==============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu.V,v
Working file: verilog/bsrc/uu/uu.V
head: 1.202
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 202;   selected revisions: 2
description:
issue unit
----------------------------
revision 1.172
date: 1995/04/05 20:35:10;  author: mws;  state: Exp;  lines: +7 -3
uu/uuprblmr9 uu/uu.V:  uuYieldsNbInR10 was on for Ifetch loopbacks, allowing
  CC to make new fill requests to NB and thus discarding loopbacks in progress.
  Test cachenasty3 accidentally noticed on a SN128WrtI.
----------------------------
revision 1.171
date: 1995/04/04 20:04:39;  author: woody;  state: Exp;  lines: +5 -2
add another copy of reset for use by prblmfrz.
==============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu_control.pim,v
Working file: verilog/bsrc/uu/uu_control.pim
head: 68.60
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 60;    selected revisions: 3
description:
----------------------------
revision 68.37
date: 1995/04/04 19:44:32;  author: woody;  state: Exp;  lines: +3121 -2103
Latest placement. Getting better, but still doesn't converge.
----------------------------
revision 68.36
date: 1995/04/03 21:57:19;  author: woody;  state: Exp;  lines: +6 -2
full placement to BOM 174.0
----------------------------
revision 68.35
date: 1995/04/03 14:20:04;  author: woody;  state: Exp;  lines: +4831 -5252
genpim.pl: remove '.noPifPack' to help toplevel placement.

pimplib.pl: more improvement on the mincut placement seed. This verision
contains >1/3 of uu. All of the bypass comparators and all of the Problem Code
Pipeline.

uu_control.pim: complete placement of uu/BOM 173.0. Trying to keep up.

success in pass3:

Atoms:                  count atom  bjt   isrc  pld   clock
       BJT Totals:      3785  25911 58156 41702 35960 17684


    Generating Gards Nets file gards/uu.slack
    Generating instance drive strength file gards/uu-pass3.strength
    Disgorging sdl file gards/uu-pass3.sdl
      Writing sdl structure: gards_47_uu_46_edif

      Congratulations!  No timing or DC Load violations!

Memory usage: 37.422MB
Exit code: 0 (Success)
================================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uuprblmr9.Veqn,v
Working file: verilog/bsrc/uu/uuprblmr9.Veqn
head: 61.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 61.15
```

```
date: 1995/04/05 20:35:16;  author: mws;  state: Exp;  lines: +13 -9
uu/uuprblmr9 uu/uu.V:  uuYieldsNbInR10 was on for Ifetch loopbacks, allowing
  CC to make new fill requests to NB and thus discarding loopbacks in progress.
  Test cachenasty3 accidentally noticed on a SN128WrtI.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uursrvduu.tdcd,v
Working file: verilog/bsrc/uu/uursrvduu.tdcd
head: 170.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 2
description:
----------------------------
revision 170.4
date: 1995/04/03 07:02:12;  author: mws;  state: Exp;  lines: +7 -7
uu/uursrvduu.tdcd cj/Makefile:
  Typo's left out GShuffleI4Mux (ex15test_0) and merge deposits
  (exresemdepitest1_0 and exresgmdepitest1_0).   Add rsrvdgsffli4mx.tst rule.
----------------------------
revision 170.3
date: 1995/04/02 01:54:35;  author: mws;  state: Exp;  lines: +3 -3
  Typo left GShuffleI and GShuffleI4Mux not checking their immediates.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uursrvduv.pla,v
Working file: verilog/bsrc/uu/uursrvduv.pla
head: 170.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 170.2
date: 1995/04/06 19:37:12;  author: mws;  state: Exp;  lines: +2 -2
Unclosed comment lost EDepI/EWithdrawI check for both
  immediates > 31.  Found by veena test uu/edepi.pl.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/yy/BOM,v
Working file: verilog/bsrc/yy/BOM
head: 26.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 61;    selected revisions: 2
description:
----------------------------
revision 25.0
date: 1995/04/03 07:15:06;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc
```

```
uu/uursrvduu.tdcd cj/Makefile:
  Typo's left out GShuffleI4Mux (ex15test_0) and merge deposits
  (exresemdepitest1_0 and exresgmdepitest1_0).   Add rsrvdgsffli4mx.tst rule.
yy/tas.pl:  Typo's prevented shufflei4mux from being recognized.
----------------------------
revision 24.1
date: 1995/04/03 07:15:00;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/yy/tas.pl,v
Working file: verilog/bsrc/yy/tas.pl
head: 1.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 24;    selected revisions: 2
description:
simple terp assembler for tstgen; supports X's in instr fields
----------------------------
revision 1.24
date: 1995/04/06 18:49:43;  author: mws;  state: Exp;  lines: +9 -8
Deposit/withdraw & copyswap had obsolete opcode-number assignments.
----------------------------
revision 1.23
date: 1995/04/03 07:10:28;  author: mws;  state: Exp;  lines: +8 -7
Typo's prevented shufflei4mux from being recognized.
=============================================================================
```